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AMENDMENTS

In the Specification

Please replace within the specification the following designated paragraphs:

Paragraph bridging pages 12-13.

Finally, within the preferred embodiment of the present invention with respect to the pair of conductor contact studs 22a and 22b, the pair of conductor contact studs 22a and 22b may be formed of conductor materials as are conventional in the art of microelectronic fabrication, including but not limited to metal, metal alloy, doped polysilicon and polycide conductor stud materials. However, as is understood by a person skilled in the art, it is preferred within the context of the present invention that the pair of conductor contact studs 22a and 22b is formed of a conductor material, and of dimensions, such as to facilitate within the context of the present invention bonding of the pair of conductor contact studs 22a and 22b with a pair of patterned conductor layers within a dielectric isolated metallization pattern subsequently laminated thereto. Thus, at least an upper portion of the conductor contact studs 22a and 22b may be formed of a thermally bondable metal (i.e., a solder) or a pressure bondable metal (for example and without limitation an indium or an indium alloy pressure bondable material), or may protrude from above the plane of the patterned planarized pre-metal dielectric layers 20a, 20b and 20c in order to facilitate bonding.

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Page 14, first paragraph.

Finally, with respect to the semiconductor integrated circuit microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 1, as is understood by a person skilled in the art, the semiconductor integrated circuit microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 1 is illustrated as a partially fabricated semiconductor integrated circuit microelectronic fabrication 24, insofar as it is desirable to fabricate upon the semiconductor integrated circuit microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 1 a dielectric isolated metallization pattern at least in part to provide a completely fabricated semiconductor integrated circuit microelectronic fabrication.

In the Claims

Please amend claim 1 and claim 11 as follows.

1. (~~A~~mended) A method for fabricating a semiconductor integrated circuit microelectronic fabrication comprising:

providing a first semiconductor substrate;

forming over the first semiconductor substrate at least one microelectronic device to form from the first semiconductor substrate a partially fabricated semiconductor integrated circuit microelectronic fabrication;

providing a second substrate;